BACHU VARUN TEJ
Second Year Postgraduate
Department of Electrical Engineering

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Education

Degree	Institution	CPI/%	Year
M. Tech (VLSI)	IIT Gandhinagar	8.11/10	2019 - Present
B. E (ECE)	R.V College of Engineering, Bengaluru	8.96/10	2013 - 2017
Class XII	Narayana Junior College, Anantapur	96.8%	2011 - 2013
Class X	Keshava Reddy Concept School, Anantapur	93.67%	2010 - 2011

Work Experience

- **Software Development Engineer, Sensors and Actuators, Department of Car Electronics and Powertrain, Mercedes Benz Research and Development, India** **[July 2017 - October 2018]**
  - Responsible for the model-based software development of sensors used for the engine functions in passenger cars. I have worked on the development of Pressure, Temperature, Level and Differential Pressure sensors in the engine.
  - I have gained experience on tools such as MATLAB, TargetLink and Tessy (Unit testing).

Publications

- S. Walia*, **Bachu Varun Tej***, J.K.Devnath*, J. Mekie, Fast and Low-Power Quantized Fixed Posit High Accuracy DNN Implementation, IEEE Transactions on VLSI Systems Brief. (Submitted) (* - equal contribution) **[May 2021]**
- P. Kumar, N. Surana, **B. V. Tej**, J. Mekie, Homo-8T: Homogeneous Energy-Efficient Mixed-VT SRAM Design Techniques for Mobile Video Decoder and Neural Network, IEEE Transactions on VLSI Systems (Submitted) **[Jun 2021]**
- C.K.Jha, **B. V. Tej**, J. Mekie, BRAD: Biased Restoring Array Dividers for Error Resilient Applications, IEEE Transactions on Circuits and Systems – II (Drafted)

Internships

- **Graduate Technical Intern, Intel, Bengaluru** **[July 2020–Dec 2020]**
  - Interning in the Graphics and Throughput Computing Hardware Engineering group.
  - Working on the 3D-Pipeline and Media Codecs for various versions of Intel GPU.
- **Engineering Intern, Graspberry, Bengaluru** **[June 2016]**
  - We as a team worked on product development of a smart lighting system using ESP 8266 Wi-Fi module. I have worked on developing the code for ESP-8266. NodeMCU was used to flash the code onto WiFi module.
- **Telecommunication Intern, BSNL, Anantapur** **[June 2015]**

Projects

- **Chip Tapeout, IIT Gandhinagar** **[Jun 2020 - Jul 2020]**
  - Designed and tested 2-stage 32-bit Synchronous processor with integrated SIPO and PISO at the input and output to decrease the number of pins required to access the processor.
  - Designed architecture level schematic for the entire processor part, which includes Synchronous and three other versions of Radiation Hardened processors.
  - Synthesized the full chip in UMC65 technology node and performed Place and Route for the design (RTL to GDS).
- **2-Stage RISC-V Processor, IIT Gandhinagar** **[Jan 2020 – Mar 2020]**
  - Design of Split Arithmetic and Logic Unit with RISC-V architecture using Bluespec System Verilog.
  - Implemented Multicycle ALU which performs Multiplication and Division using successive addition and subtraction. Flags are provided to stall the pipeline.
  - Working on the design of Approximate multipliers and dividers, which are expected to be more energy efficient compared to exact units. This project is being done under the supervision of Dr. Joycee Mekie.
- **Layout on Cadence, IIT Gandhinagar** **[Dec 2019]**
  - Designed Layouts of 6T,8T SRAM cells and mirror adder circuits.
  - Layout was made in Cadence Layout editor and DRC, LVS and PEX was done using Calibre tool.
- **Radiation Hardened 13T and 14T SRAM, IIT Gandhinagar** **[Oct 2019-Nov 2019]**
  - Designed 13T and 14T SRAM with improved writing speed, reduced power consumption compared with standard 12T SRAM in Cadence. It is designed for high radiation affected applications.
- **3X3 NOC Router using Verilog, IIT Gandhinagar** **[Sep 2019]**
- **Hybrid Method of Analysis of Shell Lens Antenna, R.V College of Engineering** **[Jan 2017-April 2017]**

Skill Summary

- **Languages:** Verilog, Python, System Verilog, Bluespec System Verilog, ALP (In order of Proficiency)
- **Tools:** Xilinx Vivado, Cadence Virtuoso, Sentaurus TCAD, MATLAB
- **Scripting:** Python, Shell, Skill, Ocean Scripting for Cadence Virtuoso

Position of Responsibilities

- Teaching Assistant for Digital Design and Embedded Systems lab at IIT Gandhinagar.
- Member of Organizing committee of CEP Social, an employee engagement team at MBRDI, Bengaluru.
- Event Organizer, 8th Mile-2016, R.V College of Engineering, Bengaluru.

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Achievements

- Secured AIR 708 (99.32 percentile) in Graduate Aptitude Test in Engineering (GATE 2019 – ECE)
- Secured AIR 34 in Indian Engineering Olympiad - 2016.